

### **REMARKS**

In the Office Action, claims 1-9, 11-17, and 19-24 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,141,769 to Petivan et al. ("Petivan"). Claims 10 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Petivan.

Applicants hereby amend claims 1-7, 11-16 and 19-22 without any intention of disclaiming any equivalents thereof. Support for the amendments to the claims may be found in the specification, for example at pages 2-3, 7-8, 21-23, 29-31, and 33. Support for the amendments to the claims may also be found in the drawings, for example in Figures 2, 6, and 8, and in the claims as originally-filed. Applicants also cancel claims 23 and 24.

Applicants respectfully submit that no new matter is entered by the present amendments to the claims. Upon entry of this paper, claims 1-22 will be pending in this application. Reconsideration is respectfully requested.

#### **Rejection of Claims 1-9, 11-17, and 19-24 Under 35 U.S.C. §102(e)**

Claims 1-9, 11-17, and 19-24 were rejected under 35 U.S.C. §102(e) as being anticipated by Petivan.

Generally, Petivan teaches a fault tolerant computer system where information is transferred among three system modules in order to detect possible system faults. (Abstract; col. 3, lines 53-60.) In Petivan, each processor directly accesses its own local memory and I/O subsystems, and does not directly access the memory or I/O subsystems located on another processor's module (See Figure 3). Specifically, Petivan discloses that:

in order to write data to an I/O device during normal synchronous system operation, all three processors synchronously direct a write request to the I/O controller local to the module that controls the target I/O device. The information to be written is actually provided to the I/O controller interface by the processor local to the target I/O device. Thus, although all three processors provide to their respective local buses the same write information, only the processor local to the target I/O device presents the information to the I/O controller interface. The subject I/O controller responds by causing the write information to be written to the target I/O device.

(Col. 5, lines 7-17. Emphasis added)

Petivan further states:

During processor writes, although all three processors synchronously request a write, only the local processor actually writes to its local I/O device. That is, only the processor local to the same module as a target I/O device can actually write to that device. An advantage of this arrangement is that a faulty processor cannot corrupt an I/O device on another module.

(Petivan, col. 9, lines 42-49.) And:

It will be appreciated that although the interconnect circuitry permits sharing of I/O information, the I/O controllers and I/O devices local to the three modules are advantageously isolated from each other. For example, the I/O devices and the I/O controller 54B are isolated from modules A and C even though transaction information is shared among modules. This sharing of transaction information facilitates error diagnoses and is necessary in order to pass information from the I/O devices to the processors. Thus, due to this isolation, the failure of an I/O device or an I/O controller associated with (or local to) one module will not corrupt data transacted on the other modules.

(Petivan, col. 9, line 61 through col. 10, line 5.)

In sum, Petivan discloses accessing a target I/O device only from the processor local to that I/O device, via an I/O controller also local to that same I/O device. Petivan explicitly isolates I/O devices on each module from processors located on other modules. Thus, in Petivan, information written to the target I/O device can only originate from the processor local to that target I/O device, and Petivan teaches away from the concept of allowing any processor to access an I/O device or I/O subsystem located on a remote module.

#### **Amended Independent Claim 1**

Applicants' amended independent claim 1 recites, in part,

- (d) a first Input/Output (I/O) subsystem, in electrical communication with the first CPU, the second CPU and the communications link, configured to compare the first information stream and the second information stream;
- (e) a second Input/Output (I/O) subsystem in electrical communication with the first CPU, the second CPU and the communications link, configured to compare the first information stream and the second information stream;
- (f) a first local mass storage device in electrical communication with both the first CPU and the second CPU, and

(g) a second local mass storage device in electrical communication with both the first CPU and the second CPU,  
wherein the first I/O subsystem is configured to selectively access the first local mass storage device based upon its comparison of the first and second information streams.

Petivan fails to teach or suggest these limitations of Applicants' amended independent claim 1. Specifically, Petivan at least does not teach or suggest a system wherein each of a first and second I/O subsystem are "in electrical communication with both the first CPU and the second CPU." Petivan also does not teach or suggest wherein each of a first and second local mass storage device are "in electrical communication with both the first CPU and the second CPU."

Instead, as described above, Petivan teaches that only the processor local to the target I/O device presents the information to the local I/O controller. This is distinguishable from the Applicants' claimed invention wherein each CPU can access I/O subsystems and mass storage devices which may be local to a different CPU (e.g. located on remote modules). Furthermore, Petivan actually teaches away from this concept, insisting that "the I/O controllers and I/O devices local to the three modules are advantageously isolated from each other." (Petivan, col. 9, lines 63-64.)

By contrast, Applicants' claimed invention facilitates communication between multiple CPUs and multiple I/O subsystems. In this fashion, when a first CPU fails, a second CPU may still access a first mass storage device local to the first CPU. Similarly, should the second CPU fail, the first CPU can access a second mass storage device local to the second CPU. Additionally, should the first mass storage device fail, the first CPU may still access information stored on the second mass storage device, even though the second mass storage device may be located on a remote module.

Accordingly, for at least these reasons, Applicants respectfully submit that amended independent claim 1 is patentable over Petivan.

**Amended Independent Claim 13**

Applicants' amended independent claim 13 recites, in part,

- (a) establishing communication between a first CPU, a communications link, a first I/O subsystem and a second I/O subsystem;
- (b) establishing communication between a second CPU, the communications link, the first I/O subsystem and the second I/O subsystem;
- ...
- (e) otherwise, storing data from the information stream on both a first mass storage device local to the first I/O subsystem and a second mass storage device local to the second I/O subsystem.

As discussed above with respect to Applicants' amended independent claim 1, Petivan at least fails to teach or suggest "establishing communication between a first CPU, a communications link, a first I/O subsystem and a second I/O subsystem" and "establishing communication between a second CPU, the communications link, the first I/O subsystem and the second I/O subsystem."

Accordingly, for at least this reason, Applicants respectfully submit that amended independent claim 13 is also patentable over Petivan.

**Amended Independent Claim 21**

Likewise, Applicants' amended independent claim 21 recites, in part,

- (e) a means for directly accessing, by the first CPU, the second local mass storage device in the event of a failure of the first local mass storage device.

As discussed above with respect to Applicants' amended independent claim 1, Petivan at least fails to teach or suggest "a means for directly accessing, by the first CPU, the second local mass storage device in the event of a failure of the first local mass storage device."

Accordingly, for at least this reason, Applicants respectfully submit that amended independent claim 21 is also patentable over Petivan.

**Dependent Claims 2-12, 14-20, and 22**

Because claims 2-12, 14-20, and 22 depend directly from one of amended independent claims 1, 13 and 21, Applicants submit that these claims are also patentable over Petivan.

Likewise, Applicants submit that the rejections to dependent claims 10 and 18 under 35 U.S.C.

§103(a) as being anticipated by Petivan are moot in light of the amendments to independent claims 1 and 13.

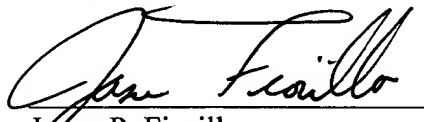
Accordingly, Applicants respectfully request that the rejection of claims 1–9, 11–17, and 19–24 under 35 U.S.C. §102(e), and the rejection of claims 10 and 18 under 35 U.S.C. §103(a), all as being anticipated by Petivan, be reconsidered and withdrawn.

### CONCLUSION

Applicants believe the above amendments and remarks to be fully responsive to all the grounds of rejection raised in the Office Action. Applicants request that the Examiner reconsider the application and claims 1–22 in light of the foregoing Amendment and Response, and respectfully submit that the pending claims are in condition for allowance. Accordingly, Applicants request withdrawal of all grounds of rejection, and allowance of claims 1–22 in due course.

If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Regards,



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